REMARKS

The Applicants respectfully request further examination and consideration in view of the arguments set forth fully below. Claims 1-66 were previously pending in this application. Within the Office Action, Claims 1-13 and 27-49 have been allowed, Claims 14, 19, 20, 25, 26, 50-54 and 60-66 have been rejected, and Claims 15-18, 21-24 and 55-59 have been objected to. Claims 2, 5, 14, 15, 27, 29, 31, 38, 44, and 50 have been amended. The majority of the claim amendments include corrections of minor typographical errors. No claims have been added or canceled. Accordingly, Claims 1-66 are currently pending.

Request for Consideration of Supplemental Information Disclosure Statements

On or about September 22, 2003, a Supplemental Information Disclosure Statement (IDS), along with an accompanying Form PTO-1449 was filed by the Applicants. The reference JP 5233426 on this Supplemental IDS has not been considered. The Applicants provide an English abstract of JP 5233426 in the **Appendix**. Also, on or about November 22, 2005, the Applicants filed a Supplemental IDS, along with an accompanying Form PTO-1449. On or about April 12, 2006, the Applicants filed a Supplemental IDS with an accompanying Form PTO-1449. To date, no consideration of these two IDS has been indicated.

The Applicants respectfully request consideration of the reference JP 5233426 on the September 22, 2003 Supplemental IDS, as well as consideration of the Supplemental IDS filed on November 22, 2005 and April 12, 2006.

Nonstatutory Double Patenting Rejections

Claims 50, 54, and 55 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claim 1 of U.S. Patent No. 6,772,274 to Estakhri (hereinafter referred to as the "'274 patent"). The Office Action states that Claim 1 of the '274 patent teaches correlation blocks but does not explicit teach overhead blocks. Then, the Office Action concludes that "[i]t would have been obvious to one of ordinary skill in the art at the time [sic] the invention to consider the correlation blocks as overhead blocks because the correlation blocks store correlation data to control operation in memory." [Office Action, page 3] The Applicants respectfully traverse this rejection.

Claim 50 of the present invention recites: "A flash memory device for storing User Data comprising a plurality of separate, independently addressable, independently programmable and

independently erasable non-volatile Physical Memory Blocks distinguishably defined by a plurality of Physical Block Addresses including: a.) a plurality of dedicated data Blocks for storing User Data only; and b.) a plurality of consecutively addressed Dedicated Overhead Blocks for storing Overhead Data only including a first Dedicated Overhead Block and a second Dedicated Overhead Block, wherein the plurality of dedicated data blocks is segregated from the plurality of dedicated overhead blocks." Claims 54 and 55 depend upon Claim 50.

In contrast, Claim 1 of the '274 patent recites: "A flash memory device having at least one flash memory array for storing incoming data sent from a host system, the flash memory device comprising: a plurality of separate, independently addressable, independently programmable and independently erasable non-volatile physical memory blocks distinguishably defined by a plurality of physical block addresses, including: a.) at least one data block for storing incoming data, a first data block defined by a first physical block address; and b.) at least one correlation block for storing correlation data within each flash memory array, a first correlation block defined by a second physical block address."

The Applicants respectfully submit that Claim 50 of the present application is patentably distinct from Claim 1 of the '274 patent. Specifically, Claim 50 does not include at least two of the limitations of Claim 1 of the '274 patent, namely:

"a.) at least one data block for storing incoming data, **a first data block defined by a first physical block address**; and

b.) at least one correlation block for storing correlation data within each flash memory array, **a first correlation block defined by a second physical block address**." (emphasis added) Further, Claim 1 of the '274 patent is patentably distinct from Claim 50 of the present application. Claim 1 of the '274 patent does not claim at least one limitation of Claim 50 of the present invention, namely, "wherein the plurality of dedicated data blocks is segregated from the plurality of dedicated overhead blocks."

Applicants respectfully submit that Claim 50 of the present invention and Claim 1 of the '274 patent are patentably distinct from each other. Further, the Applicants respectfully submit that one skilled in the art would not consider correlation blocks of the '274 patent to be overhead blocks of the present invention. For at least these reasons, the Applicants request that the double patenting rejections as to Claims 50, 54 and 55 be withdrawn.

Rejections Under 35 U.S.C. § 102

A. Conley

Claims 50, 60-63 and 65 have been rejected under 35 U.S.C. 102(e) as being anticipated by Conley et al., U.S. Patent No. 6,426,893 (hereinafter "Conley"). The Applicants respectfully traverse this rejection.

Claim 50 recites a flash memory device for storing user data that includes a plurality of separate, independently addressable, independently programmable and independently erasable non-volatile physical memory blocks distinguishably defined by a plurality of physical block addresses. The plurality of physical block addresses include a plurality of dedicated data blocks for storing user data only and a plurality of consecutively addressed dedicated overhead blocks for storing overhead data only. The plurality of consecutively addressed dedicated overhead blocks include a first dedicated overhead block and a second dedicated overhead block. Further, the plurality of dedicated data blocks is segregated from the plurality of dedicated overhead blocks.

Conley does not teach at least three limitations recited in Claim 50 of the present invention. Conley does not teach:

- a plurality of dedicated data blocks for storing user data only
- a plurality of consecutively addressed dedicated overhead blocks for storing overhead data only including a first dedicated overhead block and a second dedicated overhead block
- the plurality of dedicated data blocks is segregated from the plurality of dedicated overhead blocks

Conley discloses a flash memory system formed of floating gate memory cells arranged in blocks as the smallest unit of memory cells that are erasable together. In Conley, error correction code (ECC), or other type of redundancy code, can be generated by a controller from user data and written into the same memory block as the user data from which it is generated. [col. 2, lines 44-45] Overhead data includes ECC [col. 1, line 40-42] Further, in Conley, FIG. 4 shows an individual memory block with capacity of 528 bytes to store both one sector of data and some overhead information about the data in the same block. [col. 7, lines 65-67, col. 8, lines 1-3]. The overhead information stored in the block along with a sector of data is information about the data itself, but does not include physical overhead information about the block or its operation. [col. 13, lines 60-64]

In contrast with Conley, the present invention teaches a plurality of dedicated data blocks for storing user data only. Dedicated data blocks do not store any overhead data. Also, the present invention teaches a plurality of consecutively addressed dedicated overhead blocks for

storing overhead data only. Dedicated overhead blocks as described in the present invention do not store user data; they only store overhead data. In Conley, the overhead data of the user data is stored in the same block as the user data. Further, in the present invention, the plurality of dedicated data blocks is segregated from the plurality of dedicated overhead blocks. The purpose of segregating dedicated data blocks from dedicated overhead blocks is to utilize memory in an efficient manner. In Conley, a block can include both user data and overhead data of the user data, but not overhead data of the block. Thus, in Conley, there is no complete segregation of user data from overhead data. [col. 2, lines 44-45, col. 7, lines 65-68, and col. 8, lines 1-3]

For at least these reasons, Claim 50 is allowable over Conley. Claims 60-63 and 65 are dependent upon the independent Claim 50. Claims 60-63, and 65 also are allowable as being dependent on an allowable base claim.

B. Iida

Claims 14, 19-20, 25, 50-54, 60-63, and 65 have been rejected under 35 U.S.C. 102(e) as being anticipated by Iida et al., U.S. Patent No. 6,625,713 B2 (hereinafter "Iida"). The Applicants respectfully traverse this rejection.

Iida discloses a memory controller for reading data stored in a nonvolatile memory that includes a number of erasable blocks containing a number of pages. A logical/physical address control table stored in a logical/physical address control table block of the nonvolatile memory is searched, read, and manipulated in the nonvolatile memory. [Abstract].

In contrast to the teachings of Iida, the method and apparatus of the present invention teaches the segregation of user data, stored in a plurality of dedicated user data blocks, from the overhead data, separately stored in a plurality of dedicated overhead data blocks, within the flash memory array while maintaining a cross reference between the overhead data and the user data. **The purpose of segregating user data from overhead data is to utilize memory in an efficient manner** when one Logical Block Address repeated more often than another Logical Block Address, or when Logical Block Addresses are used at an equal rate or at variable rates. The present invention discloses a flash memory system maps a non-volatile memory medium into a plurality of independently addressable, independently programmable and independently erasable memory blocks including a plurality of dedicated data blocks and a plurality of dedicated overhead blocks. The dedicated overhead blocks comprise a first dedicated overhead block and a second dedicated overhead block. Each of the dedicated overhead blocks is mapped into a

plurality of overhead pages. Each of the overhead pages is mapped into a plurality of overhead segments. The same set of segment addresses is used for each overhead page.

Iida does not teach at least three limitations recited in Claim 50 of the present invention. Iida does not teach:

- a plurality of dedicated data blocks for storing user data only
- a plurality of consecutively addressed dedicated overhead blocks for storing overhead data only including a first dedicated overhead block and a second dedicated overhead block
- the plurality of dedicated data blocks is segregated from the plurality of dedicated overhead blocks

Contrary to what the Office Action states, Iida does not teach that overhead data is segregated from user data within the flash memory array. The Office Action admits that in Iida, overhead data can include data such as "logical address 005, flag 0" but fails to recognize that the main data blocks, such as Block 2 of FIGs. 14A and 14B, in Iida also can include redundant portions which contain user data such as logical addresses and control table flags. For instance, in FIGs. 14A and 14B, Block 2 includes main data with user data (logical address 0001, with a control table flag 0).

Also, the Office Action erroneously states that Fig. 7 of Iida shows overhead blocks 0-1 being segregated from data blocks n-1 and n [Office Action, page 12]. In fact, the user blocks n-1 to 2 of Iida cannot be considered designated user blocks as disclosed in the present invention. As shown in Figs. 7D and 7E, the user blocks include overhead data in the redundant portion, including but not limited to logical address fields, data ECC fields, etc. Therefore, Iida's user blocks contain overhead data and cannot be considered designated user blocks which store only user data. Therefore, Iida does not teach, suggest, or disclose a segregation of a plurality of user data stored in designated user data blocks from a plurality of overhead data stored in designated overhead data blocks.

The independent Claim 14 is directed to a method of data storage within a flash memory comprising the steps of mapping a non-volatile memory medium within the flash memory into a plurality of independently addressable, independently programmable and independently erasable memory blocks including a plurality of dedicated data blocks and a plurality of dedicated overhead blocks comprising a first dedicated overhead block and a second dedicated overhead block, wherein the plurality of the dedicated data blocks and the plurality of dedicated overhead blocks are segregated; mapping each of the plurality of dedicated overhead blocks into a plurality of consecutively addressed overhead segments, wherein the plurality of segments within each

dedicated overhead block are addressed according to an identical set of distinct segment addresses, each segment comprising a physical address register and a flag field; and correlating the first dedicated overhead block to a first group of Virtual Logical Block Addresses including a first Virtual Logical Block Address; wherein user data and overhead data are segregated in separate memory blocks, such that the user data are stored only in the plurality of dedicated data blocks and the overhead data are separately stored only in the plurality of dedicated overhead blocks. As described above, Iida does not teach that overhead data is segregated from user data within the flash memory array. Further, Iida does not teach that user data only is stored in the plurality of dedicated data blocks. Also Iida does not teach that overhead data only is stored in the plurality of dedicated data blocks. For at least these reasons, the independent Claim 14 is allowable over the teachings of Iida.

Claims 19, 20, and 25 are dependent upon the independent Claim 14. As discussed above, the independent Claim 14 is allowable over the teachings of Iida. Accordingly, Claims 19, 20 and 25 are allowable as being dependent upon an allowable base claim, and are now in condition for allowance.

The independent Claim 50 is directed to a flash memory device for storing user data comprising a plurality of separate, independently addressable, independently programmable and independently erasable non-volatile physical memory blocks distinguishably defined by a plurality of physical block addresses, including a plurality of dedicated data blocks for storing user data only and a plurality of consecutively addressed dedicated overhead blocks for storing overhead data only including a first dedicated overhead block and a second dedicated overhead block, wherein the plurality of dedicated data blocks is segregated from the plurality of dedicated overhead blocks. As described above, Iida does not teach, hint, or disclose at least three limitations of Claim 50. For at least these reasons, the independent Claim 50 is allowable over the teachings of Iida.

Claims 51-54, 60-63 and 65 are dependent upon the independent Claim 50. As discussed above, the independent Claim 50 is allowable over the teachings of Iida. Accordingly, Claims 51-54, 60-63 and 65 also are allowable as being dependent on an allowable base claim.

Rejection Under 35 U.S.C. § 103

Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida as applied to claim 50 above, and further in view of applicant's admitted prior art, the current specification pages 2-12 and Figs. 1-6 (hereinafter AAPA). The Applicants respectfully disagree.

Claim 64 depends from the independent Claim 50. As discussed above, Claim 50 is allowable over Conley and Iida. Accordingly, Claim 64 is also allowable as being dependent upon an allowable base claim.

Claims 26 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida as applied to claims 50 or 14 above, and further in view of Tanaka, U.S. Patent No. 6,466,177 B1 (hereinafter "Tanaka"). The Applicants respectfully disagree.

Tanaka teaches a control method of nonvolatile semiconductor memory including an one time PROM ("OTP") in a part of its memory region, which is capable of writing a mark data reliably preventing erroneous writing, etc. in the OTP region and clearly maintaining the boundary between a written region and a non-written region, and hence reliably storing irreversible changes of state. Tanaka does not teach a flash memory device with a plurality of consecutively addressed dedicated overhead blocks, which is segregated from the plurality of user data blocks. **Accordingly, neither Iida, Tanaka, nor their combination teaches a flash memory device with a plurality of consecutively addressed dedicated overhead blocks, which is segregated from the plurality of overhead data from the plurality of user data in separate memory blocks in the flash memory array.**

Claim 26 depends from the independent Claim 14. As discussed above, Claim 14 is allowable over Iida. Accordingly, Claim 26 is allowable as being dependent upon an allowable base claim.

Claim 66 depends from the independent Claim 50. As discussed above, Claim 50 is allowable over Conley and Iida. Accordingly, Claim 66 is allowable as being dependent upon an allowable base claim.

Claim Objections

Claims 15-18, 21-24, and 55-59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 15-18 and 21-24 depend from independent Claim 14. As discussed above, the independent Claim 14 is allowable over the teachings of Iida. Accordingly, Claims 15-18, and 21-24 are also allowable as being dependent upon an allowable base claim.

Claims 55-59 depend from the independent Claim 50. As described above, the independent Claim 50 is allowable over the teachings of Conley and Iida. Accordingly, Claim 55-59 are also allowable as being dependent upon an allowable base claim.

Conclusion

For the reasons given above, Applicant respectfully submit that the Claims 1-66 are in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, the Examiner is encouraged to call the undersigned at (408) 530-9700 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: 5-26-06

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CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

HAVERSTOCK & OWENS LLP

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